## REMARKS

Applicants have amended their claims in order to further clarify the definition of various aspects of the present invention. Specifically, Applicants are canceling original claims 1-28, and are adding new claims 29-54 to the application. All of claims 29-54 are directed to a method of manufacturing a semiconductor device, with claim 29 being the sole newly added independent claim.

Claim 29 recites that this method includes providing a substrate having, inter alia, a main surface and a plurality of product forming areas arranged in a matrix with spaces therebetween, on the main surface, and providing a plurality of semiconductor chips having a main surface, a back surface opposite the main surface and electrode pads formed on the main surface; mounting the plurality of semiconductor chips on the product forming areas, and, after the mounting step, treating the main surface of the substrate by plasma; providing a molding die, and, after the treating step, arranging the substrate in the molding die with the plurality of semiconductor chips positioned in the cavity of the molding die and the plurality of product forming areas facing the cavity; and after so arranging the substrate, block molding a resin enclosure sealing the semiconductor chips and plurality of product forming areas, and thereafter cutting the resin enclosure and the substrate along a periphery of each of the product forming areas.

Claims 30 and 31, dependent respectively on claims 29 and 30, respectively recites that the cavity of the molding die has two sides opposed to each other, with a gate formed on one side and an air vent formed on the other side, and wherein in

the block molding step the resin is injected into the cavity from the gate to the air vent; and recites that in the treating step by plasma, impurities remaining on the main surface of the substrate are removed. Claims 32 and 33, dependent respectively on claims 30 and 32, respectively recites that the main surface of the substrate is roughened in the treating step by plasma, and recites that the substrate is comprised of resin. Claims 34-36, dependent respectively on claims 30, 34 and 35, respectively recites that the resin enclosure includes a plurality of fillers, recites a volume content of the plurality of fillers in the resin enclosure, and recites that the plurality of fillers are comprised of silica fillers.

Claims 37 and 38, dependent respectively on claims 30 and 37, respectively recites that in the mounting step the electrode pads of the semiconductor chips are electrically connected with connecting electrodes of corresponding product forming areas of the substrate; and recites that in the mounting step, the substrate is heat treated. Claims 39 and 40, dependent respectively on claims 30 and 39, respectively recites that in the block molding step a peripheral space of the cavity is provided between the product forming areas and the air vent, with a width of the peripheral space being larger than a width of spaces between the plurality of product forming areas in plan view; and recites the same subject matter set forth in claim 31.

Claims 41 and 42, dependent respectively on claims 39 and 41, respectively recites the same subject matter set forth in claim 32, and recites that the substrate is comprised of resin; and claims 43-45, dependent respectively on claims 39, 43 and 44, respectively expressly sets forth subject matter recited in claims 34-36. Claims 46 and 47, dependent respectively on claims 39 and 46, respectively expressly recites subject matter set forth in claim 37, and recites subject matter set forth in

claim 38. New claim 48, dependent on claim 37, recites the same subject matter expressly set forth in claim 37, but is dependent on claim 29.

Claim 49, dependent on claim 29, recites that the treating step is performed to increase wettability to the substrate of the resin, of the resin enclosure, used in the step of block molding. Claims 50 and 51, each dependent on claim 49, respectively recites that the wettability of the resin, to the substrate, is sufficiently increased by the treating step by plasma so as to dislodge voids during the block molding; and recites that this wettability is sufficiently increased so as to dislodge voids, during the block molding, that are behind the semiconductor chips in the direction of flow of the resin during the block molding. Claims 52-54, dependent respectively on claims 51, 49 and 29, recite that the treating step by plasma uses an oxygen or argon gas.

In connection with the presently submitted claims, note, for example, paragraphs [0018] and [0019] on pages 7 and 8, and paragraphs [0069 - 0081] on pages 19-26, of Applicants' Substitute Specification submitted with the Preliminary Amendment filed January 28, 2002, in the above-identified application. Note also Fig. 3 and the corresponding description in connection therewith, in paragraph [0062] of the aforementioned Applicants' Substitute Specification.

The statement by the Examiner in the first paragraph on page 2 of the Office Action mailed January 8, 2003, that Figs. 23A-26B should be designated by a legend such as --Prior Art-- "because only that which is old is illustrated", is respectfully traversed. That is, it is respectfully submitted that the content of Figs. 23A-26B does not illustrate "only that which is old". To the contrary, it is respectfully submitted that the subject matter of Figs. 23A-26B had been provided to

show matters, which were not publicly known prior to the present invention, but which were originally considered by the present inventors, and, based thereon, the present inventors developed the present invention. That is, while the subject matter of Figs. 23A-26B provide a basis for explanation of the present invention, they do not illustrate that which is old. In view thereof, it is respectfully submitted that Applicants need not designate Figs. 23A-26B by a legend such as --Prior Art--.

The requirement by the Examiner for a proposed drawing correction or corrected drawings in reply to the Office Action mailed January 8, 2003, to avoid abandonment of the application, is noted. It is respectfully submitted that this traverse of the requirement to designate Figs. 23A-26B by the legend -- Prior Art-- constitutes a complete response to the issue raised by the Examiner in connection with the drawings, and that a proposed drawing correction or corrected drawings are not required to avoid abandonment of the application.

The statement by the Examiner that the objection to the drawings will not be held in abeyance, is noted. Applicants are not requesting that the objection to the drawings be held in abeyance; rather, Applicants are respectfully traversing the objection to the drawings, and respectfully request reconsideration and withdrawal of such objection.

Applicants respectfully submit that all of the claims now presented for consideration by the Examiner satisfy all requirements of 35 USC §112, second paragraph, and, in particular, are not indefinite.

The question by the Examiner, in connection with the previously considered claims, as to how one side of a flat substrate can face another side, is noted. The present claims recite that the back surface of the substrate is "opposite" the main

surface; and that a back surface of the semiconductor chips is "opposite" the main surface thereof. It is respectfully submitted that the recitations as to surfaces being opposite each other are sufficiently definite so as to satisfy requirements of the second paragraph of 35 USC § 112.

Moreover, with respect to the contention by the Examiner in the last paragraph on page 2 of the Office Action mailed January 8, 2003, the present claims do not use the term "many", with respect to the fillers mixed with the resin. In view thereof, basis for rejection of claims under the second paragraph of 35 USC § 112, set forth in the last paragraph on page 2 of the Office Action mailed January 8, 2003, is moot.

Applicants respectfully submit that all of the claims now presented for consideration by the Examiner patentably distinguish over the teachings of the references applied by the Examiner in rejecting claims in the Office Action mailed January 8, 2003, that is, the teachings of the U.S. patents to Tsuruta, No. 6,200,121, to Wensel, No. 5,963,792, and to Hsu, et al., No. 6,338,813, under the provisions of 35 USC §103.

It is respectfully submitted that these references as applied by the Examiner would have neither taught nor would have suggested such a method of manufacturing a semiconductor device as in the present claims, including, inter alia, wherein, after the mounting step of mounting the plurality of semiconductor chips on the plurality of product forming areas of the substrate, a main surface of the substrate is treated by plasma; and, thereafter, the substrate (having the plurality of semiconductor chips mounted thereon) is arranged in a molding die and thereafter the step of block molding a resin enclosure sealing the plurality of semiconductor

chips and product forming areas is performed, by injecting resin into the cavity, with the resin enclosure and substrate thereafter being cut along a periphery of each of the product forming areas of the substrate. See claim 29.

More specifically, it is respectfully submitted that the teachings of the applied references do not disclose, nor would have suggested, such method as in the present claims, including wherein in the treating step by plasma, the main surface of the substrate is roughened (note claims 32 and 41), and/or in this treating step impurities remaining on the main surface of the substrate are removed (see claims 31 and 40).

Furthermore, it is respectfully submitted that the teachings of these applied references would have neither disclosed nor would have suggested such a method of manufacturing a semiconductor device as in the present claims, including the above-referred-to treating step by plasma, and wherein this treating step is performed so as to increase wettability to the substrate of the resin, of the resin enclosure, used in the step of block molding (see claim 49); more specifically, wherein this wettability is sufficiently increased so as to dislodge voids during the block molding (see claim 50); even more specifically, wherein this wettability is sufficiently increased so as to dislodge voids, during the block molding, that are behind the semiconductor chips in the direction of flow of the resin during the block molding (see claim 51).

In addition, it is respectfully submitted that these references do not disclose, nor would have suggested, such method as in the present claims, including specifically the plasma treatment of the substrate after the mounting step and prior to arranging the substrate in the molding die, particularly to increase wettability of

the resin to the substrate and dislodge voids, with the invention including additional features as in the remaining, dependent claims, including (but not limited to) the molding die used, with injection of resin during the block molding step, as in claim 30; and/or wherein a peripheral space of the cavity is provided with a peripheral space having a width larger than a width of spaces between the plurality of product forming areas in plan view (see claim 39); and/or wherein the mounting step includes electrically connecting the electrode pads of the semiconductor chips with connecting electrodes of corresponding product forming areas (see claims 37 and 48); and/or wherein the plasma treatment uses an oxygen or argon gas (see claims 52-54).

The present invention is directed to a technique particularly suitable for manufacture of semiconductor devices using block molding by transfer molding. In the manufacture of semiconductor devices, one technique is to mount a plurality of semiconductor chips on a main surface of a substrate, block-molding the mounted semiconductor chips on the substrate with one resin enclosure, and then separating the plurality of semiconductor chips from each other by cutting the resin enclosure and the substrate (with, for example, a single semiconductor chip or stacked semiconductor chips) into respective devices.

However, as found and investigated by the Applicants, and as shown in Figs. 23A to 26B and described in the corresponding description in paragraphs [0004] to [0009] on pages 2-4 of Applicants' Substitute Specification, there arises a specific problem when block transfer molding is used in forming the plurality of semiconductor devices in one resin enclosure. That is, in performing the transfer molding, the flow of the resin 67A along the main surface of the semiconductor chip

61 is resisted by the semiconductor chip 61. Therefore, the resin flowing along the main surface of the chip runs slower than the resin 67A flowing along the side surfaces of the semiconductor chip 61 (see Figs. 24A and 24B). For this reason, voids 67B tend to be generated at positions where the resin 67A flowing along the main surface of the semiconductor chip 61 meets the resin 67A flowing along the side surfaces of the semiconductor chip 61 (see Figs. 25A and 25B). Particularly troublesome are voids 67C remaining at positions hiding behind the semiconductor chips 61 with respect to the injecting direction S of the resin 67A (see Figs. 26A and 26B). These voids, e.g., voids 67C, are a factor that reduces yield of semiconductor devices.

This problem of voids is even greater when a great amount of filler (80% or more, for example) is added to the molding resin for, e.g., purposes of reducing warpage due to the cure shrinkage of the molding resin, to facilitate the dicing process, or for providing a more compatible thermal expansion coefficient of the resin to that of the semiconductor chip. That is, in including a large amount of filler, a thixotropic property cannot be used to remove/avoid voids.

Against this background, the present inventors turned their attention to the wettability of the resin 67A to the main surface of the substrate, and based thereon, have achieved the present invention which overcomes the problems of voids. Note paragraph [0014] on page 6 of Applicants' Substitute Specification. That is, Applicants have found that voids in the resin, during the block transfer molding, becomes more easily removed from a main surface of a substrate in a step of transfer molding, by a plasma treatment enhancing wettability of the resin to the main surface of the substrate, after mounting the semiconductor chips on the

substrate. That is, as described, for example, from paragraphs [0067] through [0070] on pages 18-20 of Applicants' Substitute Specification, during the mounting procedure the substrate is heated and impurities such as fats, oils and organic solvents are outgassed so as to contaminate the main surface of the substrate. Performing the plasma treatment removes impurities, such as fats and oils; and, moreover, can roughen the surface of the substrate, all increasing wettability thereof. Since these impurities have been removed, the resin flowing along the side surfaces of the semiconductor chip 10 is allowed to easily enter positions, e.g., behind the semiconductor chips with respect to the injecting direction S of the resin 24A (see Figs. 14A and 14B). As a result, the voids 24B generated at the positions where the resin 24A flowing along the main surface of the semiconductor chip 10 meets the resin 24A flowing along the side surfaces of the semiconductor chip 10 are dislodged, and the voids thus dislodged are able to easily move in response to the flow of the resin in the resin injecting process. Therefore, the voids do not remain at positions behind the chips. Thus, problems due to such voids can be avoided.

Tsuruta discloses a process for molding semiconductor chips, and a molding die used therein. The process includes steps of preparing a circuit panel having plural conductive patterns formed on an insulating layer and plural semiconductor chips mounted on the circuit panel and electrically connected to the plural conductive patterns, respectively; accommodating the semiconductor chips mounted on the circuit panel in a cavity of a molding die having a gate extending along one of peripheral lines defining the cavity; supplying melted synthetic resin through the gate into the cavity so as to fill the vacant space of the cavity therewith; solidifying the melted synthetic resin; and cutting the large piece of synthetic resin so that the

semiconductor chips are sealed in small pieces of synthetic resin, respectively. See column 3, lines 29-45.

It is respectfully submitted that this patent does not disclose, nor would have suggested, the problem addressed by Applicants, of voids in block molding a plurality of chips within a single resin block which is later cut, particularly voids formed behind chips in the direction of resin flow; and would have neither disclosed nor would have suggested the solution to this problem of voids as discovered by Applicants, of utilizing the plasma treatment after mounting and prior to block molding.

It is respectfully submitted that the secondary references as applied by the Examiner would not have rectified the deficiencies of Tsuruta, such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art.

Wensel discloses an encapsulant molding technique for chip-on-board encapsulation, wherein an oxidizable metal layer is patterned on a carrier substrate and a top surface of the oxidizable metal layer is oxidized to facilitate removal of unwanted encapsulant material deposited during the molding operation. This patent discloses forming a single encapsulation around a single element. In discussing the state of the art with respect to the chip-on-board encapsulation, this patent discloses that various methods have been devised to prevent excess channel encapsulant from adhering to the carrier substrate. This patent discloses that one such method described in U.S. Patent No. 5,542,171 treats a predetermined portion of the surface of the carrier substrate over which the mold channels will reside to prevent the excess encapsulant material thereon from adhering to the carrier substrate, this

patent teaching selectively contaminating the surface portion with an ink or a polymer. Wensel goes on to describe that such a technique as in No. 5,542,171 would not be applicable to FR-4 substrates (flame retardant epoxy glass laminate), which require a cleaning step, such as plasma cleaning, just before encapsulation to remove unwanted organic compounds in order to obtain sufficiently strong adhesion between the encapsulant material and the FR-4 substrate; Wensel discloses that the plasma cleaning would also remove the ink or polymer. Wensel then goes on to disclose application of the oxidizable metal layer on a specific portion of the carrier substrate, with this oxidizable metal layer then being oxidized to form a metal oxide layer, which does not adhere to most encapsulant materials. Note column 1, lines 8-15; column 2, lines 23-49; and column 3, lines 2-35.

It is noted that Wensel is concerned with providing an encapsulant for individual semiconductor chips, wherein excess encapsulant material is removed by stripping the encapsulant from a surface of the substrate adjacent the chip. Compare with Tsuruta, disclosing a block molding technique wherein, for example, the individual chip size packages would then be cut off from each other after block molding. It is respectfully submitted that one of ordinary skill in the art concerned within the procedure set forth in Tsuruta, of providing block molding, would not have looked to the teachings of Wensel as applied by the Examiner.

It is respectfully submitted that there would have been no motivation, as required under 35 USC §103, for combining the teachings of Tsuruta and of Wensel, as applied by the Examiner.

The Examiner contends that Wensel discloses that cleaning is required for FR-4 substrates prior to encapsulation to remove unwanted organic compounds and

thus obtain sufficiently strong adhesion between the encapsulant material and the FR-4 substrate. However, taking Wensel, et al. as a whole, this patent requires a cleaning step to obtain sufficiently strong adhesion in (individually forming) structure having the individual chips. It is respectfully submitted that only through hindsight use of the present invention, which, of course, is improper under 35 USC §103, would one of ordinary skill in the art have used the teachings of Wensel together with the teachings of Tsuruta, as applied by the Examiner.

Moreover, it is again emphasized that according to the present invention voids can be avoided by increasing wettability, by the recited plasma treatment. Note particularly claims 49-51. It is respectfully submitted that neither of Tsuruta nor Wensel, either alone or in combination, would have disclosed or suggested the problem addressed by the present invention, of voids occurring based upon flow patterns of the resin during the block transfer molding; and would have neither disclosed nor would have suggested the solution to this problem, of utilizing the plasma treatment after mounting but prior to block molding, to dislodge such voids and thus avoid such void problems.

It is respectfully submitted that the Examiner must take into account the present invention as a whole, including the problem addressed (discovered) by Applicants and source thereof, and solution thereto. Particularly noting the problem addressed by Applicants and source thereof, it is respectfully submitted that the teachings of the applied references clearly do not disclose, nor would have suggested, the problem or source thereof. Moreover, taking the present invention as a whole, including the problem addressed and source thereof, it is respectfully submitted that the teachings of the applied references would have neither disclosed

nor would have suggested the present invention.

Again, attention is specifically directed to claims 49-51. Particularly with respect to these claims, it is respectfully submitted that the teachings of the applied references would have neither disclosed nor would have suggested the problem, source of the problem and solution thereto, as in the present invention.

The contention by the Examiner in the paragraph bridging pages 3 and 4 of the Office Action mailed January 8, 2003, that it would have been obvious to clean the substrate taught by Tsuruta prior to encapsulation to remove unwanted organic compounds, and thus obtain sufficiently strong adhesion between the encapsulant material and FR-4 substrates, is noted. It is noted, however, that Tsuruta does not appear to disclose FR-4 substrates; accordingly, basis for the conclusion by the Examiner to utilize the teachings of Wensel to achieve strong adhesion between the encapsulant material and the FR-4 substrate in the process of Tsuruta is not understood. Reference by the Examiner to "glass fiber reinforced substrate (a.k.a. FR4)" is noted. However, it is respectfully submitted that there are many types of glass reinforced substrates, and that not all glass fiber reinforced substrates are FR-4 substrates.

Again, it is emphasized that the present invention solves a problem neither disclosed nor suggested by the applied prior art; and, moreover, the present invention also describes a source of such problem. This provides a basis for patentability of the present invention, especially as recited in claims 49-51, for example.

It is respectfully submitted that the remaining secondary reference applied by the Examiner, Hsu, et al., would not have rectified the deficiencies of the teachings

of Tsuruda and of Wensel, such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art. Hsu, et al. discloses a molding method for a BGA semiconductor chip package, the molding method being described most generally from column 1, line 58 to column 2, line 6. According to this method, the molding die includes at least two runners connected to the molding cavity, with the two lines of bonding pads of each chip being substantially perpendicular to the flowing direction of the molding compound during transfer molding. This avoids the problem of bonding wire movement, since the bonding wires are substantially parallel to the flowing direction of the molding compound. See column 3, lines 5-11. This patent further discloses that the described molding method can be used to encapsulate an array of stacked chips to form a stacked chip package device. See column 4, lines 1-5. Note also column 4, lines 22-29.

Even assuming, arguendo, that the teachings of Hsu, et al. were properly combinable with the teachings of Tsuruta and of Wensel, it is respectfully submitted that the combined teachings of these references do not disclose, nor would have suggested, the presently claimed method, including the plasma treatment after mounting and prior to block molding, and advantages achieved thereby, or other aspects of the present invention as discussed previously.

In view of the foregoing comments and amendments, reconsideration and allowance of all claims presently in the application are respectfully requested.

To the extent necessary, applicant's petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing

of this paper, including extension of time fees, to Deposit Account No. 01-2135 (501.40695X00) and please credit any excess fees to such deposit account.

Respectfully submitted,

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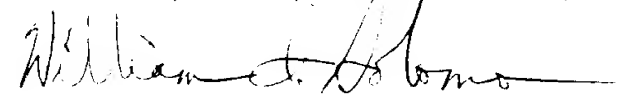

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